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HOGUE, DENNIS A	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/673,775	MABUCHI, KEIJI	
	Examiner	Art Unit	
	DENNIS HOGUE	2622	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 January 2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *6-11,13-18 and 20-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *6-11,13-18 and 20-27* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *7/11/2008* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This is the third Office Action based on the 10/673,775 application filed 9/29/2003. Claims 6, 11, 13, 18, 20, and 25 as amended, claims 7-10, 14-17, 21-24, and 26 as previously presented, and new claim 27, are currently pending and have been considered below. Claims 1-5, 12, and 19 have been cancelled.

Continued Examination Under 37 CFR 1.114

2. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 1/14/2009 has been entered.

Response to Amendment

3. In view of the amendments to claims 20 and 26, the rejections of claims 20-26 under USC 112 are withdrawn.

Response to Arguments

4. Applicant's arguments with respect to claims 6-11, 13-18, and 20-27 have been considered but are moot in view of the new ground(s) of rejection.

5. Regarding applicant's argument on page 10 of the amendment received on 1/14/2009, which states that a layer of a pixel structure cannot be a node, and cannot have a capacitance, the argument is not persuasive. Anything conductive can be a node, and anything conductive has a capacitance. In fact, any real electrical node has a capacitance with respect to any other real electrical node.

Remarks

6. The specification of the applicant, at least as the examiner understands it, appears to disclose two inventions. The first invention is an image sensor wherein the substrate voltage is lowered during readout. Two embodiments are disclosed: an embodiment for an image sensor having a well for each row of pixels (called "first example" in the spec); and an embodiment for an image sensor having a single well for all of the pixels (called "first example" in the spec). In the examiner's opinion, Nakagawa (JP-2000-022126) teaches the inventive concept of lowering the substrate voltage at the time of signal transfer. The second invention disclosed is an image sensor wherein the substrate voltage is varied during exposure to expand the dynamic range (called "third example" in the spec). In the examiner's opinion, Murakami et al. (US Patent 6,486,460) and Morimoto (US Patent 5,729,287) teach this inventive concept. The Applicant should strongly consider these references, as they are very relevant.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 6, 7, 11, 13, 14, 18, 20, 21, 25, and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Murakami et al. (US Patent 6,486,460) in view of Raynor et al. (US Patent 7,375,752).

Regarding claim 6, Murakami et al. teach a solid-state complementary metal-oxide semiconductor type image pickup device (solid-state image sensing device 1 which is a CMOS sensing means, col. 5 lines 36-39), comprising: a semiconductor substrate (P- semiconductor region 221 is a substrate, see Fig. 19A) having a well region formed thereon (P semiconductor region 222 is a well region, Fig. 19A); and a pixel unit (multiple sensing means 2, Fig. 8) having a plurality of pixels on the semiconductor substrate (multiple sensing means 2 is arrayed in a matrix, col. 5 lines 24-26, see Fig. 8; the pixels are the individual sensor elements of Fig. 8), each pixel in the pixel unit including (a) a photoelectric conversion element formed in said well region to receive light and produce a signal charge in accordance with an amount of the received light (N semiconductor region 224 and P semiconductor region 222 form a photodiode, see Fig. 19A; as is well known in the art, the photodiode converts photons into electric charges); (c) a node connected to the photoelectric conversion element (a node connects the N semiconductor region 224 to drive transistor 212, see Fig. 19A), the node having a capacitance (any real electrical node has a capacitance with respect to any other real electrical node); and (d) a voltage control unit to apply a variable substrate bias voltage to said well region upon the read out of the signal charge by said readout section (the substrate voltage is varied during the exposure period so as to increase the dynamic range of the captured image, col. 5 lines 43-48; Fig. 9 shows an embodiment where the substrate voltage is varied during exposure, having two distinct substrate voltages that are applied; embodiments wherein the substrate voltage is varied in unequal time amounts, four different equally spaced levels, four logarithmically

spaced voltage levels, and continuously varied are shown in Figs. 11, 13, 15, and 17 respectively; note that in all cases a different substrate voltage is applied when the pixel is not being exposed; therefore, the substrate voltage is varied, and a particular substrate voltage is applied when the pixel is read out; the substrate voltage is also applied to the well region because they are in contact, see Fig. 19A). However, Murakami et al. do not teach (b) a readout section formed in said well region to read out the signal charge produced by said photoelectric conversion element at a predetermined readout timing. That is, Murakami et al. teach the common three transistor (3T) CMOS pixel, which does not feature a transfer gate.

Raynor et al. teach a CMOS image sensor having the common four transistor (4T) pixel structure (see Fig. 4). Note that this structure differs from the three transistor structure (as shown in Fig. 1) in that a transfer gate transistor has been added (transistor M4). As is well known in the art, the pixel is read out by a timing signal Vtx applied to the gate of the transfer transistor M4. Raynor et al. teach that advantages of the 4T pixel structure over the 3T structure are increased sensitivity and that the 4T structure allows for a rolling shutter application (col. 1 line 58 to col. 2 line 9).

Therefore, it would be obvious to one of ordinary skill in the art to combine the transfer gate of Raynor et al. with the imaging device of Murakami et al. so that the sensitivity of the device could be improved and a rolling shutter application could be supported. This would increase the quality of the images captured by the camera device.

Regarding claim 7, Murakami et al. in view of Raynor et al. teaches the complementary metal-oxide semiconductor type solid-state image pickup device according to claim 6, wherein said plurality of pixels are arranged in a two-dimensional array on said semiconductor substrate (Murakami et al.: multiple sensing means 2 is arrayed in a matrix, col. 5 lines 24-26, see Fig. 8; the pixels are the individual sensor elements of Fig. 8).

Regarding claim 11, Murakami et al. in view of Raynor et al. teaches the complementary metal-oxide semiconductor type solid-state image pickup device according to claim 6, wherein said solid-state image pickup device each pixel also includes a pixel transistor connected to said photoelectric conversion element through said node for converting the signal charge read out from said photoelectric conversion element into an electric signal and outputting the electric signal to a signal line (Murakami et al. teach drive transistor 212, see Fig. 19A; Raynor et al. teach amplifying transistor M1, see Fig. 4; both of these transistors are pixel transistors for converting the signal charge read out from said photoelectric conversion element into an electric signal and outputting the electric signal to a signal line).

Regarding claims 13, Murakami et al. teach a complementary metal-oxide semiconductor type solid-state image pickup device (solid-state image sensing device 1 which is a CMOS sensing means, col. 5 lines 36-39), comprising: a semiconductor substrate (P- semiconductor region 221 is a substrate, see Fig. 19A) having a well region formed thereon (P semiconductor region 222 is a well region, Fig. 19A); and a pixel unit (multiple sensing means 2, Fig. 8) having a plurality of pixels on the semiconductor substrate (multiple sensing means 2 is arrayed in a matrix, col. 5 lines 24-26, see Fig. 8; the pixels are the individual sensor elements of Fig. 8), each pixel in the pixel unit including (a) a photoelectric conversion element formed in said well region to receive light and produce a signal charge in accordance with an amount of the received light (N semiconductor region 224 and P semiconductor region 222 form a photodiode, see Fig. 19A; as is well known in the art, the photodiode converts photons into electric charges); (c) a node connected to the photoelectric conversion element (a node connects the N semiconductor region 224 to drive transistor 212, see Fig. 19A), the node having a capacitance (any real electrical node has a capacitance with respect to any other real electrical node); and (d) a voltage control unit to apply a substrate bias voltage to said well region and change the substrate bias voltage during a storage period of the signal charge by said photoelectric conversion element (the substrate voltage is varied during the exposure period so as to increase the dynamic range of the captured image, col. 5 lines 43-48; Fig. 9 shows an embodiment where the substrate voltage is varied during exposure, having two distinct substrate voltages that are applied; embodiments wherein the substrate voltage is varied in unequal time amounts,

four different equally spaced levels, four logarithmically spaced voltage levels, and continuously varied are shown in Figs. 11, 13, 15, and 17 respectively; note that in all cases a different substrate voltage is applied when the pixel is not being exposed; therefore, the substrate voltage is varied, and a particular substrate voltage is applied when the pixel is read out; the substrate voltage is also applied to the well region because they are in contact, see Fig. 19A). However, Murakami et al. do not teach (b) a readout section formed in said well region to read out the signal charge produced by said photoelectric conversion element at a predetermined readout timing. That is, Murakami et al. teach the common three transistor (3T) CMOS pixel, which does not feature a transfer gate.

Raynor et al. teach a CMOS image sensor having the common four transistor (4T) pixel structure (see Fig. 4). Note that this structure differs from the three transistor structure (as shown in Fig. 1) in that a transfer gate transistor has been added (transistor M4). As is well known in the art, the pixel is read out by a timing signal Vtx applied to the gate of the transfer transistor M4. Raynor et al. teach that advantages of the 4T pixel structure over the 3T structure are increased sensitivity and that the 4T structure allows for a rolling shutter application (col. 1 line 58 to col. 2 line 9).

Therefore, it would be obvious to one of ordinary skill in the art to combine the transfer gate of Raynor et al. with the imaging device of Murakami et al. so that the sensitivity of the device could be improved and a rolling shutter application could be supported. This would increase the quality of the images captured by the camera device.

Regarding claim 14, Murakami et al. in view of Raynor et al. teaches the complementary metal-oxide semiconductor type solid-state image pickup device according to claim 13, wherein said plurality of pixels are arranged in a two-dimensional array on said semiconductor substrate (Murakami et al.: multiple sensing means 2 is arrayed in a matrix, col. 5 lines 24-26, see Fig. 8; the pixels are the individual sensor elements of Fig. 8).

Regarding claim 18, Murakami et al. in view of Raynor et al. teaches the complementary metal-oxide semiconductor type solid-state image pickup device according to claim 13, wherein said solid-state image pickup device each pixel also includes a pixel transistor connected to said photoelectric conversion element through said node for converting the signal charge read out from said photoelectric conversion element into an electric signal and outputting the electric signal to a signal line (Murakami et al. teach drive transistor 212, see Fig. 19A; Raynor et al. teach amplifying transistor M1, see Fig. 4; both of these transistors are pixel transistors for converting the signal charge read out from said photoelectric conversion element into an electric signal and outputting the electric signal to a signal line).

Regarding claim 20, Murakami et al. teach a method to drive a solid-state image pickup device (solid-state image sensing device 1 which is a CMOS sensing means, col. 5 lines 36-39) including (a) a semiconductor substrate (P- semiconductor region 221 is a substrate, see Fig. 19A) having a well region formed thereon (P semiconductor region 222 is a well region, Fig. 19A) and (b) a pixel unit (multiple sensing means 2, Fig. 8) including a plurality of pixels on the semiconductor substrate (multiple sensing means 2 is arrayed in a matrix, col. 5 lines 24-26, see Fig. 8; the pixels are the individual sensor elements of Fig. 8), each pixel in the pixel unit including (i) a photoelectric conversion element formed in said well region to receive light and produce a signal charge in accordance with an amount of the received light (N semiconductor region 224 and P semiconductor region 222 form a photodiode, see Fig. 19A; as is well known in the art, the photodiode converts photons into electric charges); (iii) a node connected to the photoelectric conversion element (a node connects the N semiconductor region 224 to drive transistor 212, see Fig. 19A), the node having a capacitance (any real electrical node has a capacitance with respect to any other real electrical node); and (iv) a voltage control means to apply a substrate bias voltage to said well region and change the substrate bias voltage during a storage period of the signal charge by said photoelectric conversion element (the substrate voltage is varied during the exposure period so as to increase the dynamic range of the captured image, col. 5 lines 43-48; Fig. 9 shows an embodiment where the substrate voltage is varied during exposure, having two distinct substrate voltages that are applied; embodiments wherein the substrate voltage is varied in unequal time amounts, four different equally spaced levels, four logarithmically

spaced voltage levels, and continuously varied are shown in Figs. 11, 13, 15, and 17 respectively), said method comprising the steps of: converting light to a signal charge (N semiconductor region 224 and P semiconductor region 222 form a photodiode, see Fig. 19A; as is well known in the art, the photodiode converts photons into electric charges); storing said signal charge during a charge storage period (the electric charges are stored in the photodiode until such time that the selection transistor 213 is turned on by signal X, see Fig. 19A); and applying a predetermined substrate bias voltage to said well region that is variable dependent upon the signal charge read out by said readout section during said readout period (the substrate voltage is varied during the exposure period so as to increase the dynamic range of the captured image, col. 5 lines 43-48; Fig. 9 shows an embodiment where the substrate voltage is varied during exposure, having two distinct substrate voltages that are applied; embodiments wherein the substrate voltage is varied in unequal time amounts, four different equally spaced levels, four logarithmically spaced voltage levels, and continuously varied are shown in Figs. 11, 13, 15, and 17 respectively). However, Murakami et al. do not teach (ii) a readout section formed in said well region to read out the signal charge produced by said photoelectric conversion element at a predetermined readout timing. That is, Murakami et al. teach the common three transistor (3T) CMOS pixel, which does not feature a transfer gate.

Raynor et al. teach a CMOS image sensor having the common four transistor (4T) pixel structure (see Fig. 4). Note that this structure differs from the three transistor structure (as shown in Fig. 1) in that a transfer gate transistor has been added (transistor M4). As is well known in the art, the pixel is read out by a timing signal Vtx applied to the gate of the transfer transistor M4. Raynor et al. teach that advantages of the 4T pixel structure over the 3T structure are increased sensitivity and that the 4T structure allows for a rolling shutter application (col. 1 line 58 to col. 2 line 9).

Therefore, it would be obvious to one of ordinary skill in the art to combine the transfer gate of Raynor et al. with the imaging device of Murakami et al. so that the sensitivity of the device could be improved and a rolling shutter application could be supported. This would increase the quality of the images captured by the camera device.

Regarding claim 21, Murakami et al. in view of Raynor et al. teaches the driving method for the complementary metal-oxide semiconductor type solid-state image pickup device according to claim 20, wherein said photoelectric conversion element is provided for each of a plurality of pixels formed in a two-dimensional array on said semiconductor substrate (Murakami et al.: multiple sensing means 2 is arrayed in a matrix, col. 5 lines 24-26, see Fig. 8; the pixels are the individual sensor elements of Fig. 8).

Regarding claim 25, Murakami et al. teach a method for driving a complementary metal-oxide semiconductor type solid-state image pickup device (solid-state image sensing device 1 which is a CMOS sensing means, col. 5 lines 36-39) including (a) a semiconductor substrate (P- semiconductor region 221 is a substrate, see Fig. 19A) having a well region formed thereon (P semiconductor region 222 is a well region, Fig. 19A); and (b) a pixel unit (multiple sensing means 2, Fig. 8) having a plurality of pixels on the semiconductor substrate (multiple sensing means 2 is arrayed in a matrix, col. 5 lines 24-26, see Fig. 8; the pixels are the individual sensor elements of Fig. 8), each pixel in the pixel unit including (i) a photoelectric conversion element formed in said well region to receive light and produce a signal charge in accordance with an amount of the received light (N semiconductor region 224 and P semiconductor region 222 form a photodiode, see Fig. 19A; as is well known in the art, the photodiode converts photons into electric charges); (iii) a node connected to the photoelectric conversion element (a node connects the N semiconductor region 224 to drive transistor 212, see Fig. 19A), the node having a capacitance (any real electrical node has a capacitance with respect to any other real electrical node); and (iv) a voltage control unit to apply a substrate bias voltage to said well region and change the substrate bias voltage during a storage period of the signal charge by said photoelectric conversion element (the substrate voltage is varied during the exposure period so as to increase the dynamic range of the captured image, col. 5 lines 43-48; Fig. 9 shows an embodiment where the substrate voltage is varied during exposure, having two distinct substrate voltages that are applied; embodiments wherein the substrate voltage is varied in unequal time amounts,

four different equally spaced levels, four logarithmically spaced voltage levels, and continuously varied are shown in Figs. 11, 13, 15, and 17 respectively), said method comprising the steps of: converting light to a signal charge (N semiconductor region 224 and P semiconductor region 222 form a photodiode, see Fig. 19A; as is well known in the art, the photodiode converts photons into electric charges); storing said signal charge during a charge storage period (the electric charges are stored in the photodiode until such time that the selection transistor 213 is turned on by signal X, see Fig. 19A); and applying a substrate bias voltage to said well region and changing the substrate bias voltage during said storage period of the signal charge by said photoelectric conversion element (the substrate voltage is varied during the exposure period so as to increase the dynamic range of the captured image, col. 5 lines 43-48; Fig. 9 shows an embodiment where the substrate voltage is varied during exposure, having two distinct substrate voltages that are applied; embodiments wherein the substrate voltage is varied in unequal time amounts, four different equally spaced levels, four logarithmically spaced voltage levels, and continuously varied are shown in Figs. 11, 13, 15, and 17 respectively). However, Murakami et al. do not teach (ii) a readout section formed in said well region to read out the signal charge produced by said photoelectric conversion element at a predetermined readout timing. That is, Murakami et al. teach the common three transistor (3T) CMOS pixel, which does not feature a transfer gate.

Raynor et al. teach a CMOS image sensor having the common four transistor (4T) pixel structure (see Fig. 4). Note that this structure differs from the three transistor structure (as shown in Fig. 1) in that a transfer gate transistor has been added (transistor M4). As is well known in the art, the pixel is read out by a timing signal Vtx applied to the gate of the transfer transistor M4. Raynor et al. teach that advantages of the 4T pixel structure over the 3T structure are increased sensitivity and that the 4T structure allows for a rolling shutter application (col. 1 line 58 to col. 2 line 9).

Therefore, it would be obvious to one of ordinary skill in the art to combine the transfer gate of Raynor et al. with the imaging device of Murakami et al. so that the sensitivity of the device could be improved and a rolling shutter application could be supported. This would increase the quality of the images captured by the camera device.

Regarding claim 26, Murakami et al. in view of Raynor et al. teaches the driving method for the complementary metal-oxide semiconductor type solid-state image pickup device according to claim 25, wherein said photoelectric conversion element is provided for each of a plurality of pixels formed in a two-dimensional array on said semiconductor substrate (Murakami et al.: multiple sensing means 2 is arrayed in a matrix, col. 5 lines 24-26, see Fig. 8; the pixels are the individual sensor elements of Fig. 8).

9. Claims 8, 15, and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Murakami et al. (US Patent 6,486,460) in view of Raynor et al. (US Patent

7,375,752) as applied to claims 7, 14, and 21 above, and further in view of Rhodes (US Patent 6,825,878).

Regarding claims 8 and 15, Murakami et al. in view of Raynor et al. teaches the complementary metal-oxide semiconductor type solid-state image pickup device according to claims 7 and 14. However, Murakami et al. in view of Raynor et al. does not teach that said well region is electrically integral in a region of said semiconductor substrate which includes all of said pixels arranged in the two-dimensional array, and a common substrate bias voltage to all of said pixels is applied to the well regions.

Rhodes teaches that all of the pixels of the pixel portion of an image sensor are formed in a single well (col. 7 lines 62-65).

Therefore, it would be obvious to one of ordinary skill in the art to combine the single well for the pixel array of Rhodes with the image sensor of Murakami et al. in view of Raynor et al. so that the complexity of the device would be reduced. This would reduce the cost of the device. That is, one of ordinary skill would recognize that it is simpler to construct a single well for all of the pixels, rather than individual wells for each pixel or a subset of pixels.

Regarding claim 22, Murakami et al. in view of Raynor et al. teaches the driving method for the complementary metal-oxide semiconductor type solid-state image pickup device according to claim 21. However, Murakami et al. in view of Raynor et al. does not teach that said well region is electrically integral in a region of said semiconductor substrate which includes all of said pixels arranged in the two-dimensional array, and a common substrate bias voltage to all of said pixels is applied to the well regions.

Rhodes teaches that all of the pixels of the pixel portion of an image sensor are formed in a single well (col. 7 lines 62-65).

Therefore, it would be obvious to one of ordinary skill in the art to combine the single well for the pixel array of Rhodes with the image sensor of Murakami et al. in view of Raynor et al. so that the complexity of the device would be reduced. This would reduce the cost of the device. That is, one of ordinary skill would recognize that it is simpler to construct a single well for all of the pixels, rather than individual wells for each pixel or a subset of pixels.

10. Claims 9, 16, and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Murakami et al. (US Patent 6,486,460) in view of Raynor et al. (US Patent 7,375,752) as applied to claims 7, 14, and 21 above, and further in view of Chi (US Patent 6,501,109).

Regarding claims 9 and 16, Murakami et al. in view of Raynor et al. teaches the complementary metal-oxide semiconductor type solid-state image pickup device according to claims 7 and 14. However, Murakami et al. in view of Raynor et al. does not teach wherein said well region is formed in an electrically isolated relationship for each row of said pixels arranged in the two-dimensional array, and an independent substrate bias voltage is applied to the cell regions for each row.

Chi teaches a CMOS image sensor (col. 3 lines 40-41) wherein a row of pixels is constructed in a single well (col. 4 lines 8-9). Having a well for each row of pixels allows

the well for each row to be individually pulsed for enhancement of the pixel dynamic range (col. 5 lines 62-65).

Therefore, it would be obvious to one of ordinary skill in the art to combine the single well for a row of pixels as taught by Chi with the image sensor of Murakami et al. in view of Raynor et al. so that the well for each row could be individually pulsed for enhancement of the pixel dynamic range. This would increase the quality of images captured by the camera.

Regarding claim 23, Murakami et al. in view of Raynor et al. teaches the driving method for the complementary metal-oxide semiconductor type solid-state image pickup device according to claim 21. However, Murakami et al. in view of Raynor et al. does not teach wherein said well region is formed in an electrically isolated relationship for each row of said pixels arranged in the two-dimensional array, and an independent substrate bias voltage is applied to the cell regions for each row.

Chi teaches a CMOS image sensor (col. 3 lines 40-41) wherein a row of pixels is constructed in a single well (col. 4 lines 8-9). Having a well for each row of pixels allows the well for each row to be individually pulsed for enhancement of the pixel dynamic range (col. 5 lines 62-65).

Therefore, it would be obvious to one of ordinary skill in the art to combine the single well for a row of pixels as taught by Chi with the image sensor of Murakami et al. in view of Raynor et al. so that the well for each row could be individually pulsed for enhancement of the pixel dynamic range. This would increase the quality of images captured by the camera.

11. Claims 10, 17, and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Murakami et al. (US Patent 6,486,460) in view of Raynor et al. (US Patent 7,375,752) as applied to claims 6, 13, and 20 above, and further in view of Merrill (US Patent 5,747,840).

Regarding claims 10 and 17, Murakami et al. in view of Raynor et al. teaches the complementary metal-oxide semiconductor type solid-state image pickup device according to claims 6 and 13, wherein said well region is a p-type well region (Murakami: P semiconductor region 222 is a well region, Fig. 19A). However, Murakami et al. in view of Raynor et al. does not teach that the substrate bias voltage is a negative voltage.

Merrill teaches a CMOS image sensor (col. 2 lines 26-28) wherein a photodiode 100 (Fig. 4) is formed in a p-well 112, 114 formed on a substrate 110 (substrate 110 may be n-type col. 4 lines 33-38). Merrill teaches that it is advantageous to reverse bias the well-substrate interface by applying a positive voltage to one layer and a negative voltage to the other layer (col. 1 lines 58-60) because the reverse biased junction prevents thermally generated carriers from diffusing from the substrate to the photodiode (col. 2 lines7-12). This improves the noise characteristics of the photodiode. Merrill further teaches that including a highly doped layer as a sub layer of the well will increase the quantum efficiency of the photodiode by deflecting photoelectrically generated charge carriers back toward the photodiode that would otherwise be lost to the substrate (col. 3 lines 30-33).

Therefore, it would be obvious to one of ordinary skill in the art to combine the highly doped well sub layer and the reverse biased well-substrate junction of Merrill with the image sensor of Murakami et al. in view of Raynor et al. so that noise characteristics and quantum efficiency would be improved. This would increase the quality of the images captured by the sensor. In such a combination, a negative voltage would be applied to the p-well and a positive voltage would be applied to the n-substrate.

Regarding claim 24, Murakami et al. in view of Raynor et al. teach the driving method for a complementary metal-oxide semiconductor type solid-state image pickup device according to claim 20, wherein said well region is a p-type well region (p-well 102). However, Murakami et al. in view of Raynor et al. does not teach that the substrate bias voltage is a negative voltage.

Merrill teaches a CMOS image sensor (col. 2 lines 26-28) wherein a photodiode 100 (Fig. 4) is formed in a p-well 112, 114 formed on a substrate 110 (substrate 110 may be n-type col. 4 lines 33-38). Merrill teaches that it is advantageous to reverse bias the well-substrate interface by applying a positive voltage to one and a negative voltage to the other (col. 1 lines 58-60) because the reverse biased junction prevents thermally generated carriers from diffusing from the substrate to the photodiode (col. 2 lines7-12). This improves the noise characteristics of the photodiode. Merrill further teaches that including a highly doped layer as a sub layer of the well will increase the quantum efficiency of the photodiode by deflecting photoelectrically generated charge carriers back toward the photodiode that would otherwise be lost to the substrate (col. 3 lines 30-33).

Therefore, it would be obvious to one of ordinary skill in the art to combine the highly doped well sub layer and the reverse biased well-substrate junction of Merrill with the image sensor of Murakami et al. in view of Raynor et al. so that noise characteristics and quantum efficiency would be improved. This would increase the quality of the images captured by the sensor. In such a combination, a negative voltage would be applied to the p-well and a positive voltage would be applied to the n-substrate.

12. Claim 27 is rejected under 35 U.S.C. 103(a) as being unpatentable over Murakami et al. (US Patent 6,486,460) in view of Raynor et al. (US Patent 7,375,752) as applied to claim 6 above, and further in view of Nakagawa (Japanese Patent Application Publication 2000-022126).

Regarding claim 27, Murakami et al. in view of Raynor et al. teaches the complementary metal-oxide semiconductor type solid-state image pickup device according to claim 6. However, Murakami et al. in view of Raynor et al. does not teach wherein the readout voltage is reduced by applying the substrate bias voltage synchronized with charge transfer.

Nakagawa teaches an image sensor wherein when the charge is transferred from the photoelectric conversion device, a lower substrate voltage is applied to the substrate than the voltage applied to the substrate prior to transferring the charges (see abstract). This reduces the voltage required at the transfer gate to transfer the charge and therefore reduces the power consumption of the device (see abstract).

Therefore, it would be obvious to one of ordinary skill in the art to combine the reduced substrate voltage at transfer of Nakagawa with the imaging device of Murakami et al. in view of Raynor et al. so that the power consumption of the device could be reduced. This would reduce heat in the sensor and also extend battery life.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to DENNIS HOGUE whose telephone number is (571) 270-5089. The examiner can normally be reached on Mon. - Thurs., 8:00 AM - 5:00 PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lin Ye can be reached on (571) 272-7372. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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/Tuan V Ho/

Primary Examiner, Art Unit 2622

DH

Examiner

3/6/2009